ESDi-XL

Comprehensive Chip-level ESD Protection Verification

Avoid Respins, Field Failures, & Over Design

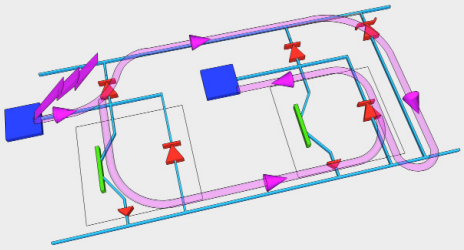
Verifying Electrostatic Discharge (ESD) protection on an IC can be challenging, and if not done correctly can lead to failures on the tester, reduced product reliability or shortened field life. Discovery of an ESD protection issue at a late stage in the design process can affect shipment dates and lead to costly and difficult rework. Field reliability issues caused by ESD protection network issues can be even more devastating.

Magwel offers a breakthrough in ESD analysis with its revolutionary ESDi-XL product. ESDi-XL thoroughly analyzes all of the pad2pad combinations in a design. Chips with large numbers of pins are analyzed extremely quickly using parallel processing and optimizations that preserve accuracy and boost speed.

ESDi-XL not only isolates and extracts the ESD network - it also identifies overstresses on core devices. Sophisticated Electronic Rule Checks (ERCs) are also performed to help remove ESD weaknesses.

ESDi-XL uses extraction and simulation engines specifically designed for ESD verification to analyze the circuit layout and protection devices. It does a better job than conventional circuit simulators because it handles snapback device models.

ESDi-XL analyzes parallel ESD device triggering for accurate current values on all discharge paths using precise extracted parasitics for the full ESD protection network. ESDi-XL also can run on schematics only for detection of ESD issues early in the product design cycle.



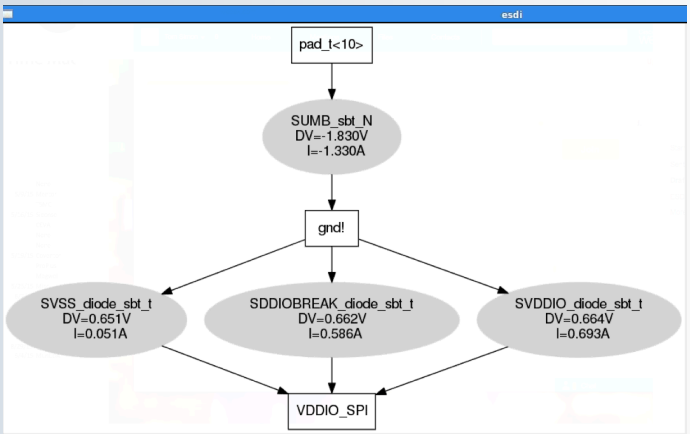
ESDi Highlights

- Runs HBM simulations on all pad2pad combinations
- Checks for over-stresses on core devices
- Schematic based ERC for early analysis results
- Supports multiple power domains and pad grouping
- Accurately extracts large power/ground nets
- Simulates currents inside ESD cells, including during snap back.
- Reports bus resistance, voltage-stress, electro-migration violations, and device burnout
- Checks for missing or undersized vias & current crowding in metal and vias

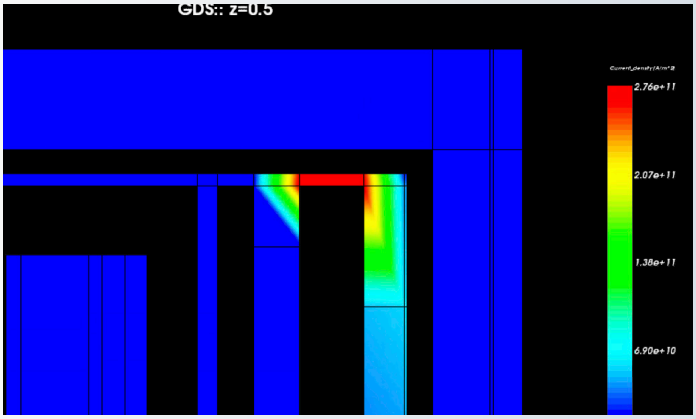
User Interface

- Ease of use with clickable results cross-linked to field view and layout
- Integrated environment with GUI, layout editor, field viewer (all cross-linked)
- EM violation visualization in layout
- Current density viewing
- Report for excessive voltage/current on core devices

Multiple Discharge Paths



Electromigration Violation



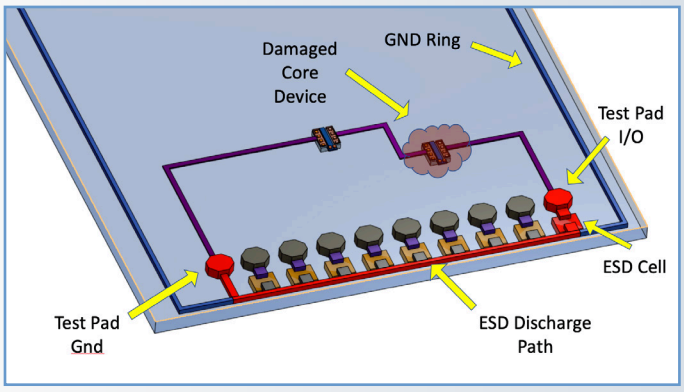
Interfaces

- Uses TLP measurement data as table model, no modeling required
- Cadence Virtuoso schematic/layout
- Auto-tagging of ESD devices, support for scalable models, self-protecting devices
- Uses ITF for setting up extraction rules

Advanced Features

- Full core checking for ESD stresses
- Sophisticated Schematic ERC checks
- Snap back device non-linear modeling
- Parallel processing for fast results
- Handles AMS and digital designs
- Full Electromigration and junction breakdown analysis
- Checks via arrays and metal lines for adequate current carrying ability

Core Checking



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