CDMi

Chip-level CDM ESD Simulation Based Verification

Avoid Respins, Yield Issues & Field Failures

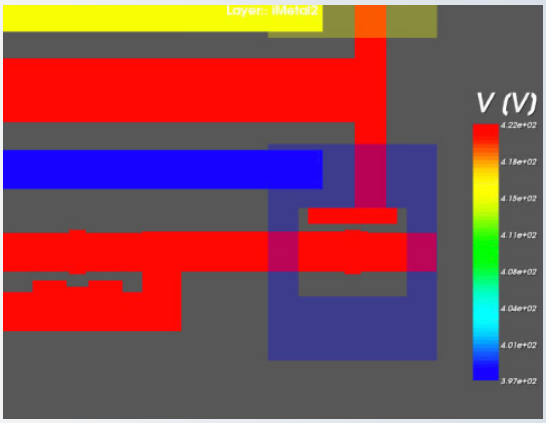
With larger die and package sizes, advanced process nodes and more automated handling of finished chips during assembly and test, CDM looms larger as a source of chip and board failure. While HBM protections are still essential, helping to reduce overall failure rates, CDM failures are an increasing concern. Predicting and accurately simulating CDM failures is not as straightforward as performing pad to pad based HBM simulations.

Magwel's CDMi uses solver based extraction to create a highly accurate model of the large nets in a design. On-chip and off-chip inductances and capacitances, including decoupling and blocking capacitances, are included. Complex current flows of stored charge through triggered devices are calculated.

Magwel's CDMi reports over-voltage, over-current, EM violations, voltages drops over meta interconnect, including vias and contacts, and voltages across devices. Dynamic simulation with support for snap back models and multiple parallel discharge paths reduces the number of false errors, making error diagnosis more efficient. These capabilities have already been field proven with Magwel's existing HBM simulation tool, ESDi®. Cross power domain checks are also performed.

Dynamic simulation is the most accurate method of understanding voltage overstress on protected devices in the IO ring and core. Magwel's FastCDM™ engine offers high performance and accurate transient results. Traditional simulation methods are too slow for larger advanced node SOCs and have difficulty with TLP models typically used to model ESD devices.

CDM Voltage Across Device Terminals



CDMi Highlights

- Chip-level dynamic CDM simulations on all pads
- Models distributed stored charge on large nets and package
- Solver based extraction of large power/ground nets
- Includes capacitive current paths, including decoupling, device and blocking caps
- Simulates currents inside ESD cells, including during snap back
- Reports bus resistance, voltage-stress, electro-migration violations, and device burnout

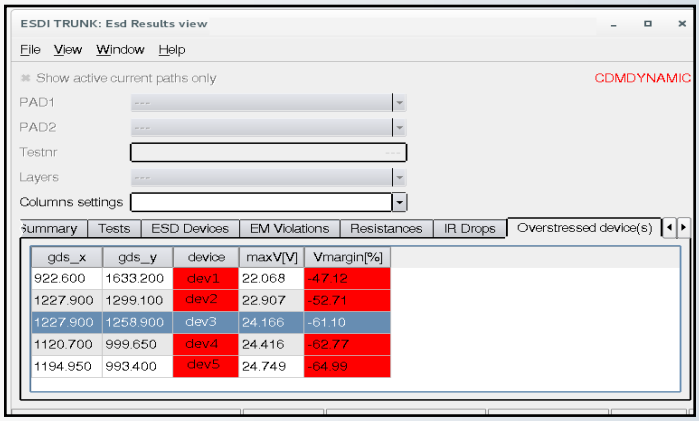
User Interface

- Ease of use with clickable results cross-linked to field view and layout
- Integrated environment with GUI, layout editor, field viewer (all cross-linked)
- EM violation visualization in layout
- Current density viewing
- Excessive voltage flagged on protected devices
- Comprehensive test reports

Advanced Features

- Transient modeling for induced currents of stored charge
- Snap back device non-linear modeling
- Parallel processing for fast results
- Handles AMS and large digital designs
- Full Electromigration and junction breakdown analysis
- Checks via arrays and metal lines for adequate current carrying ability

CDM Overstress Violation Report

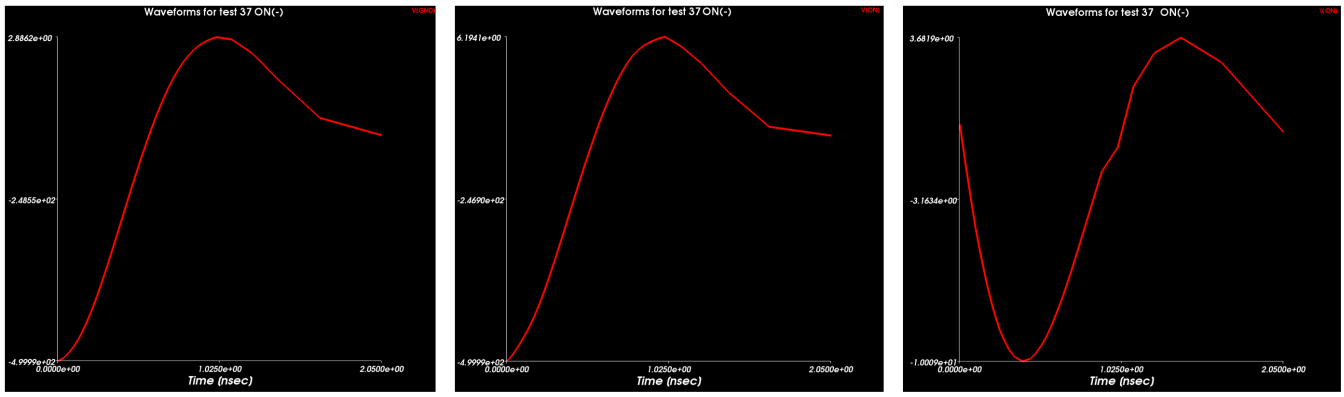


gds_x	gds_y	device	maxV[V]	Vmargin[%]
922.600	1633.200	dev1	22.068	-47.12
1227.900	1299.100	dev2	22.907	-52.71
1227.900	1258.900	dev3	24.166	-61.10
1120.700	999.650	dev4	24.416	-62.77
1194.950	993.400	dev5	24.749	-64.99

Interfaces

- Uses TLP measurement data for table model, no modeling required
- Cadence Virtuoso
- Auto-tagging of ESD devices, support for scalable models, self-protecting devices
- Uses ITF for setting up extraction rules

Voltage and Current During CDM Test



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