



PTM-TR

Power Transistor Transient Simulation Solution

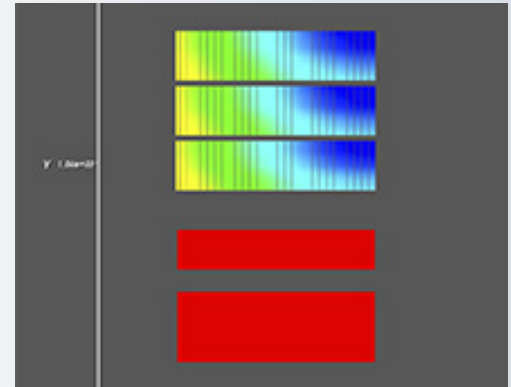
Increase Productivity - Avoid Re-spins, Field Failures, & Over Design

High performance power transistors are frequently used in power management IC's, where switching behavior is extremely important. However, due to their large distributed gate and active area structure, achieving optimal switching performance and minimizing switching power loss can be challenging. Designers need accurate extraction and modeling tools for power transistors with complex wide metal and 3D current flows.

PTM-TR integrates with Cadence Virtuoso ADE to fully model 3D current flow and non-uniform distributed device switching in power transistors that can affect performance in power conversion circuits. The PTM-TR's Fast3D models are derived from a 3D field solver model of layout and allow co-simulation of power devices to predict: signal propagation in large gate nets, non uniform switching of device fingers, as well as shoot-through current and current-crowding.

To assist in optimization, PTM-TR can simulate high and low-side devices together with drivers and test benches including load models and parasitic inductances so that dead-time and switching power loss can be minimized in the familiar Virtuoso ADE environment with parametric and process corners capabilities.

PTM-TR's user interface also offers detailed visualization of power transistor transient behavior. PTM-TR improves reliability with EM violation and current density reporting for power devices during circuit transients.



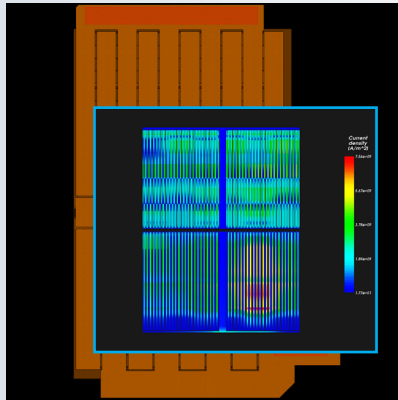
PTM-TR Field Viewer shows non-uniform switching I_{ds} in a NMOS/PMOS low and high side pair at a specified time during switching

PTM-TR Capability Highlights

- Virtuoso ADE based co-simulation solution for power transistors in conversion circuits
- Helps minimize dead-time and power loss in DC-to-DC converters and switching power supplies
- Analyzes signal propagation delays in gate nets
- Simulates non-uniform switching of device fingers
- Highlights shoot-through currents, IR drops and current-crowding in metal
- Determines Miller coupling to the Gate of a fast dV/dt transient in the Drain

Comprehensive Power Device Transient Simulation

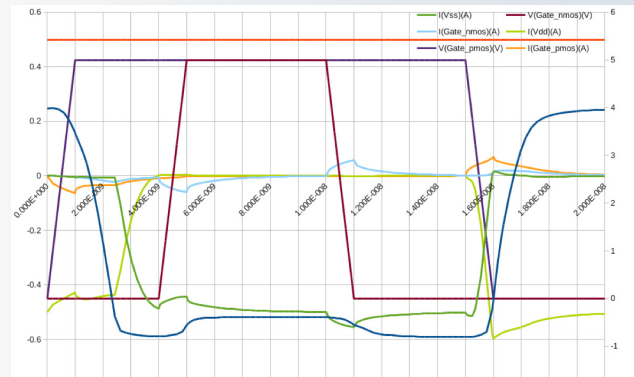
PTM-TR combines 3D field-solver based extraction technology with power device models to create Fast3D models for transient analysis of power device circuits within Cadence Virtuoso ADE. All angle meshing delivers high accuracy in modeling complex 3D currents.



PTM power device visualization showing Current density

Features

- Co-simulation in Virtuoso ADE with user test benches at all process corners
- True 3D simulation accuracy with state-of-the-art sparse matrix iterative solvers
- Efficient mesh generator for large, complex 3D structures containing transistors with channel widths of several meters
- Powerful 2D and cross-cut viewing of current densities and electric potentials. Display of I_{ds} , V_{ds} and voltage drops along wide channels, plus textual output in csv files
- Supports wedge-shaped, rounded & other non-Manhattan layouts, metal slotting, and circular and diamond shaped vias
- Simulation of active devices with Virtuoso Spectre simulator using industry standard device models
- Supports CMOS, DMOS (lateral and vertical) & IGBT power devices, honeycomb, serpentine and other layout architectures



Reported I, V behavior over time

Power Transistor Modeling Suite

PTM is part of a comprehensive family of tools available from Magwel for modeling all aspects of power transistor behavior and performance. Designing competitive power devices requires a thorough understanding of the timing, transient and electro-thermal behavior of power transistors.

PTM - Power Transistor Modeler

Using its 3D all angle mesh solver, PTM extracts $R_{ds(on)}$ for power transistors. It reports and graphically shows current densities, power dissipation and electromigration violations.

PTM-GD - Gate Delay

Switching in power transistors depends on the RC characteristics of the metal and poly gate interconnect. PTM-GD uses its highly accurate solver to extract distributed RC models for the gate interconnect and device capacitance. This information is used to predict turn-on/off time for power transistors that have very large gate widths.

PTM-TR - Transient

Solving transient behavior in power transistors requires understanding both the metalization and the device physics. PTM-TR produces Fast3D models for Virtuoso ADE co-simulation to provide a complete picture of dynamic device switching behavior.

PTM-ET - Electro-Thermal

PTM-ET combines interconnect and device joule heating with other heat sources and sinks to determine device thermal behavior. PTM-ET concurrently and dynamically models device thermal and electrical performance for devices in their packaging using stimulus to provide an accurate view during circuit operation over time.

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