PTM

3D Solver Based Power Transistor Device and Interconnect Modeling

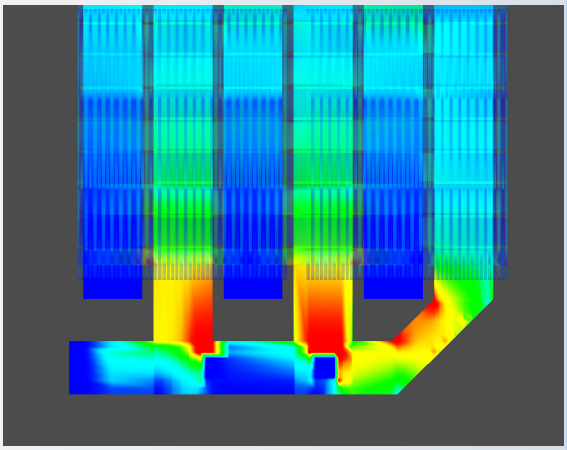
Increase Productivity - Avoid Respins, Field Failures, & Over Design

Today, power transistor designers use a combination of hand calculations and test-chips to optimize the layout of their devices for Rdson (DC on-resistance), and satisfy electro-migration rules and mean-time-to-failure requirements. Traditional 2D and 2.5D layout extractors are not suitable for power transistors due to the non-uniform complex 3D current flows. The lack of accurate extractors often leads designers to over-design to avoid expensive design iterations.

PTM's integrated environment combines a state-of-the-art 3D field solver, an easy-to-use results viewer featuring cross linked reports and a field viewer. Incorporating an all-angle edge-based 3D mesher and 64-bit numerical solvers, PTM extracts Rdson in large power transistor arrays by computing detailed non-uniform current distributions in metal & poly interconnect and vias while including bond wires in the simulation.

The tool offers extremely fast simulation on standard Linux workstations with Rdson results matching silicon typically within 2%-5%.

PTM reports and displays current densities and electro-migration rule violations on the layout. Current density and voltage distributions can be viewed in 2D or cross-cut formats. Designers can focus on potential trouble spots by locally increasing mesh density for better accuracy. Designers also have full control of terminal placement and excitation, including test benches with Voltage Controlled Current Sources (VCVS) to help with high precision sense device design.



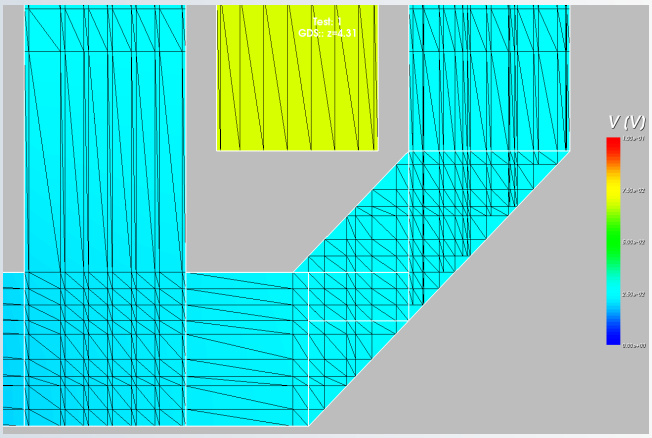
PTM calculates and reports current densities and power dissipation in power devices

PTM Capability Highlights

- Extract Rdson in large power transistor arrays including metal/poly interconnect, vias, oxide & gate capacitance, and bond wires
- Identify current crowding, electro-migration & IR drop issues on layout
- Explore layout alternatives such as terminal placement with integrated editor
- Extract R and power dissipation values for all layers in a single run
- Analyze sensitivity to process & temperature variations
- Non-linear channel model improves LDO design
- VCVS helps with designing high precision sense devices
- Silicon proven accuracy and predictability

Advanced Meshing

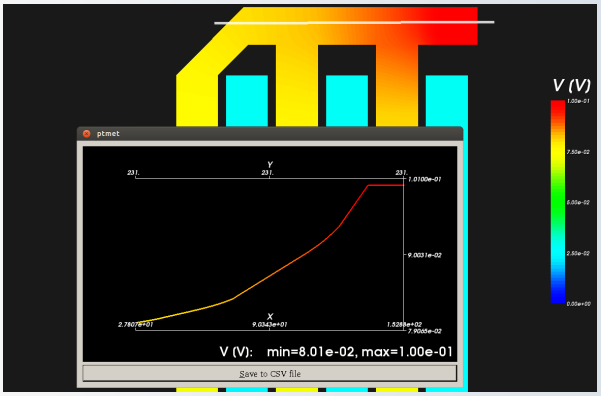
PTM uses a highly accurate all-angle mesher to achieve superior results with non-rectilinear geometry. This produces significantly better accuracy for source and drain resistance extraction. PTM excels with circular, serpentine and 45 degree angle layout shapes.



Curved shapes are accurately meshed

Features

- True 3D simulation accuracy with state-of-the-art sparse matrix iterative solvers
- Efficient mesh generator for large, complex 3D structures containing transistors with channel widths of several meters
- Powerful 2D and cross-cut viewing of current densities and electric potentials. Display of Ids, Vds and voltage drops along channels, plus textual output in csv files
- Supports wedge-shaped, rounded & other non-Manhattan layouts, metal slotting, and circular and diamond shaped vias
- Linear and non-linear modeling of active area to account for Vds, Vgs and Vbe (bipolar) bias-variation over the array
- Supports CMOS, DMOS (lateral and vertical) & IGBT power devices, honeycomb, serpentine and other complex layout architectures



Field View supports cross-cut plots

Power Transistor Modeling Suite

PTM is part of a comprehensive family of tools available from Magwel for modeling all aspects of power transistor behavior and performance. Designing competitive power devices requires a thorough understanding of the timing, transient and electro-thermal behavior of power transistors.

PTM - Power Transistor Modeler

Using its 3D all-angle mesh solver, PTM extracts Rdson for power transistors. It reports and graphically shows current densities, power dissipation and electromigration violations.

PTM-GD - Gate Delay

Switching in power transistors depends on the RC characteristics of the metal and poly gate interconnect. PTM-GD uses its highly accurate solver to extract distributed RC models for the gate interconnect and device capacitance. This information is used to predict turn-on/off time for power transistors that have very large gate widths.

PTM-TR - Transient

Solving transient behavior in power transistors requires understanding both the metalization and the device physics. PTM-TR produces Fast3D models for Virtuoso ADE co-simulation to provide a complete picture of dynamic device switching behavior.

PTM-ET - Electro-Thermal

PTM-ET combines interconnect and device joule heating with other heat sources and sinks to determine device thermal behavior. PTM-ET concurrently and dynamically models device thermal and electrical performance for devices in their packaging using stimulus to provide an accurate view during circuit operation over time.

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