ESDi

Chip-level ESD-Network Layout Extraction & Simulation Based Verification

Avoid Respins, Field Failures, & Over Design

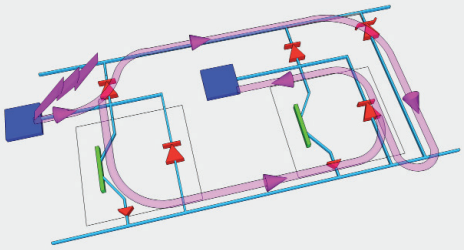
Verifying the Electrostatic Discharge (ESD) protection network on an IC can be challenging, and if it is not done correctly it can lead to failures on the tester, reduced product reliability or shortened field life. Discovery of an ESD protection network issue such as parasitic junction triggering at a late stage in the design process can affect shipment dates and lead to costly and difficult rework. Field reliability issues caused by ESD protection network issues can be even more devastating.

Magwel offers a breakthrough in ESD analysis with its revolutionary ESDi product. ESDi thoroughly analyzes all pin combinations in a design for comprehensive ESD event protection. Chips with large numbers of pins are analyzed extremely quickly using parallel processing and optimizations that preserve accuracy and boost speed.

ESDi automatically isolates and extracts the ESD network, including all supply nets. ESDi checks for potential break down or triggering of parasitic junctions and parasitic Bipolar devices.

Unlike rule based tools, ESDi uses extraction and simulation engines specifically designed for ESD verification to analyze the circuit layout and protection devices. It also does a better job than conventional circuit simulators because they do not handle snapback modeling.

ESDi analyzes multiple ESD device triggers per event which provides accurate current values on all discharge paths using precise extracted parasitics for the full ESD protection network. User specified rules are used to look for violations which are reported through the user interface or graphically.



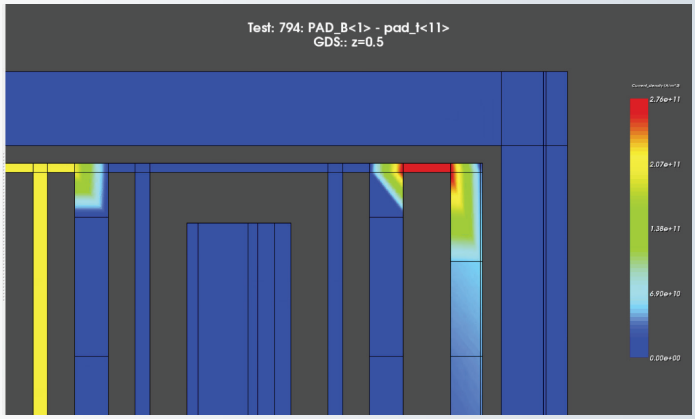
ESDi Highlights

- Runs static HBM simulations on all pad2pad combinations
- Supports multiple power domains and pad grouping
- Extracts large power/ground nets
- Looks for parasitic junction or Bipolar device breakdown or turn-on
- Checks to see if protected devices are triggered before protection devices
- Simulates currents inside ESD cells, including during snap back.
- Reports bus resistance, voltage-stress, electro-migration violations, and device burnout
- Checks for missing or undersized vias
- Checks for current crowding in metal and vias

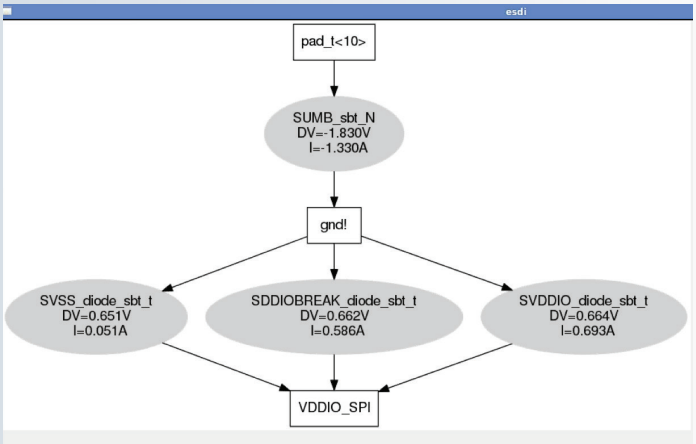
User Interface

- Ease of use with clickable results cross-linked to field view and layout
- Integrated environment with GUI, layout editor, field viewer (all cross-linked)
- EM violation visualization in layout
- Current density viewing
- Excessive voltage flagged on protected devices
- Test Reports

Electromigration Violation



Multiple Discharge Paths



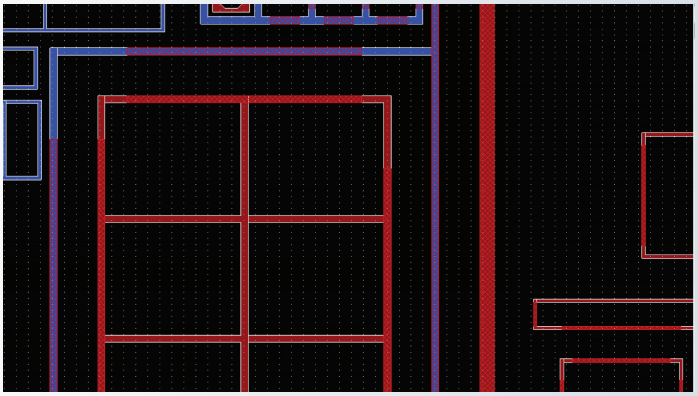
Interfaces

- Uses TLP measurement data for table model, no modeling required
- Cadence Virtuoso
- Auto-tagging of ESD devices, support for scalable models, self-protecting devices
- Uses ITF for setting up extraction rules

Advanced Features

- Identifies parasitic junctions and substrate Bipolar junctions
- Snap back device non-linear modeling
- Parallel processing for fast results
- Handles AMS and large digital designs
- Full Electromigration and junction breakdown analysis
- Checks via arrays and metal lines for adequate current carrying ability

N+ and P+ Parasitic Junctions



Magwel NV
Vital Decosterstraat 44, bus 27
3000 Leuven, Belgium
+32 16 43 81 13

www.magwel.com