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Project: **CODESTAR**

Project Number: IST-2001-34058

Work Package: 0

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Title: Project Presentation

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Abstract

An overview of CODESTAR project is given. The project partners, the key issues and the project's main goals are addressed. Also the technical approach and the expected achievements and impacts are given.

Project Presentation

Contract number: **IST-2001-34058**

Project acronym: **CODESTAR**

Project name: **Compact modeling of on-chip passive structures at high frequencies**

Key Action, Action line: **IV.8.2**

Project logo:



Website: <http://www.imec.be/codestar>

List of participants:

NAME	SHORT NAME	COUNTRY
IMEC	IMEC	B
Ghent University	INTEC	B
Austriamicrosystems	AMS	A
Philips	PHILIPS	NL
Technische universiteit Eindhoven	TUE	NL
Universitatea 'Politehnica' din Bucuresti centrul De inginerie electrica asista de calculator	LMN	RO

Total cost: 2.603.960 EURO

Commission funding: 1.711.730 EURO

Project main goals: During the **CODESTAR** project software dedicated for on-chip passives and interconnects patterns is developed. Starting from the layout description, the result of the **CODESTAR** code is an equivalent net list taking into account the detailed electrodynamics of passive on-chip structures. This netlist can be loaded into a compact model simulator (e.g. SPICE) (**Figure 1**).

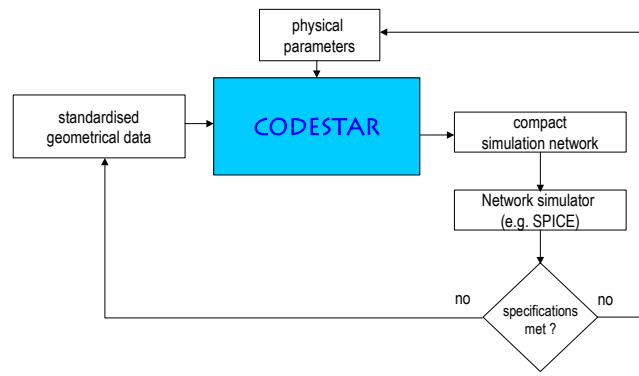


Figure 1: Codestar as a part of a design cycle for on-chip structures

Key issues: The main goal of the **CODESTAR** project is the development of a code dedicated for the electromagnetic simulation of passive on-chip structures resulting in a small simulation network. First a detailed analysis of the test structure is carried out using an electromagnetic field solver. The outcome of the field solver is a full description of the detailed characteristics of the passive structure. A descriptive equivalent net list will be too large to be useful and therefore a systematic reduction of the net list must be done (i.e. reduced-order modelling). The resulting compact equivalent lumped-element model is inserted back into the full design scheme and the design cycle can be pursued. Parallel fabrication, characterisation and evaluation of dedicated test structures is carried out, in order to validate the **CODESTAR** code. The matching between experimental and **CODESTAR** simulation results is the measure of the project success.

Technical approach: A critical part of a passive on-chip design is submitted to a detailed analysis by the **CODESTAR**-code.

- The first part of the project deals with this detailed analysis of the critical structure using an electromagnetic field solver. Three types of field solvers are considered and compared, being the finite-difference-time-domain solver, the finite-integration solver and a recently developed lattice-gauge solver.
- In general, this net list will be too large to be useful for inclusion in the design database and therefore a systematic reduction of the net list must be carried out i.e. application of reduced-order modelling (ROM). After having obtained a sufficiently

compact equivalent lumped-element model (using original and efficient ROM techniques), the result is inserted back into the full design scheme and the interconnect design cycle will be continued. The emphasis of this work will be on the development of new techniques like the Laguerre-SVD and the two-step Lanczos technique and their connection with the different field solving techniques.

- Parallel with this code development process, dedicated test structures are designed and evaluated to validate the **CODESTAR** code. The test-cases will attempt to capture the complexity of realistic interconnect structures, will highlight the limits of present CAD tools and allow to assess the enhancements brought by the new tool created in this project.

Expected achievements/impact:

CODESTAR will accelerate the design of passive on-chip structures like inductors, capacitors and critical parts of the interconnect layout (net lists) by executing the following steps:

- The **CODESTAR** code reads the geometrical and physical information of the design problem taking into account the material properties of the design.
- The software solves the electromagnetic fields and the charge transport in each sub-structure of the design using order reduction techniques.
- **CODESTAR** converts the result into an equivalent net list that is next submitted to order-reduction techniques to obtain an equivalent net list of lower complexity valid in prescribed frequency ranges, with an imposed accuracy.
- Starting from the layout description, the result of the **CODESTAR** code is an equivalent net list of passive elements and interconnect patterns taking into account the detailed electrodynamics of passive on-chip structures, that can be loaded into a compact model simulator (e.g. SPICE)

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